

Dr B R AMBEDKAR NATIONAL INSTITUTE OF TECHNOLOGY JALANDHAR

G T Road By Pass, Jalandhar-144008, Punjab (India) (An Institute of National Importance)

Advertisement Notice

Admission to PhD (Full-Time) under Visvesvaraya PhD Scheme Phase -II, Round - II

Applications are invited for admission to PhD (Full-Time) Programme under Visvesvaraya PhD Scheme Phase-II. The Broad areas of Research, Eligibility Criteria, Selection Procedure, Teaching Assistantship-cum-Scholarships etc. are given in this advertisement.

How to apply: The link to fill the online application form can be accessed through Institute website www.nitj.ac.in. An application fee of Rs.1000/- (Rs.500/- for SC/ST/PWD candidates) is required to be paid online. The candidates are required to apply online and there is no requirement to send the Hard Copy of the application form to the Institute. Application fee shall not be refunded in any case.

Last date for submission of online application form is 13/07/2025.

For more details, the candidates are advised to visit the Institute website www.nitj.ac.in for updates. All updates regarding this Advertisement will be updated on the Institute website only. All candidates are advised to visit the Institute website regularly.



Dr B R AMBEDKAR NATIONAL INSTITUTE OF TECHNOLOGY, JALANDHAR

G T Road By Pass, Jalandhar-144008, Punjab (India) (An Institute of National Importance)

Admission to PhD (Full-Time) Programme under Visvesvaraya PhD Scheme Phase -II

A) Broad Areas of Research

Sr.	Department	(Broad Areas of Research)	Number	
No.	Email address of		of Seats	
	HOD			
01	Electronics &	ESDM: Semi Conductor, Material Technology,	02	
	Communication	Artificial Intelligence, Circuits Design and		
	Engineering	Fabrication		
02	Information Technology	ITES: Artificial Intelligence, Blockchain, Quantum 01		
		Computing		
The above seats may to shift the both branches in case of non-availability of the suitable candidates.				

B) Eligibility Criteria

1.1 The eligibility criteria for the minimum educational qualification will be as under:

- Master's Degree in Engineering/Technology in the relevant area of research along with Bachelor's Degree in appropriate branch of Engineering/Technology with a first class or minimum 60% marks (or CGPA of 6.5 on 10-point scale) in the qualifying examination. GATE is mandatory.
- Direct Ph.D. admission is also available in case of candidate with B Tech/B.E./BS (4 year) with a
 CGPA of 8.5 and above on a 10-point scale or 80% aggregate from a Centrally Funded Technical
 Institute (CFTI). All such candidates must be GATE qualified. Number of credit courses to be
 cleared will be 24 credits before comprehensive examination.

• Department Specific (Information Technology):

- (i) Master's degree in Engineering/Technology in the relevant area of research with minimum CGPA of 6.5 on a 10-point scale or equivalent in the qualifying examination. The candidates having B. Tech degree in other than CSE/IT must be GATE qualified in CS/IT/Data Science and Artificial Intelligence discipline
- (ii) Bachelor's degree in Engineering/Technology from a Centrally Funding Technical Institutes (CFTI) with minimum CGPA of 8.5 or above on a 10-point scale or equivalent in the qualifying examination. In such cases, the candidates have to fulfil the requirement of minimum of 24 credits of course work.

1.2 The ongoing/dropped PhD students are not eligible.

C) Details of Visvesvaraya PhD Scheme Phase –II:

03 Full-Time PhD seats are available under the Visvesvaraya PhD Scheme Phase –II funded by Ministry of Electronics and IT (MeitY) in the Department of Electronics & Communication Engineering and Information Technology. The details are as under:

Title of the Project	Visvesvaraya PhD Scheme Phase –II, Round -II			
Funding Agency	Ministry of Electronics and IT (MeitY).			
Number of PhD seats	Total Seats	Nan	ne of Branch	Number of Seats
	`		etronics and nmunication Engineering	02
		Information Technology 01		01
	The above seats may to shift the both branches in case of non availability of the suitable candidates.			
Position	PhD fellowship			
Fellowship Amount and other Benefits	Fellowship		Rs. 38750/- (1 st and 2 nd yea Rs. 43750/- (3 rd , 4 th and 5 th	,
	Reimbursen of Rent	ent	As per Funding Agency N	orms
	Research Contingency grant		Rs. 1,20,000/ year	
	Other/detailed Terms and Conditions: As Visvesvaraya PhD Scheme Phase –II, Round - II fur by Ministry of Electronics and IT (MeitY).			
	Link: https://p	<u>hd.di</u>	gitalindiacorporation.in/hor	<u>me</u>
Eligibility Criteria and Admission Procedure	As per the PhD Full-Time (under Institute Fellowship)			
Broad Areas of Research	ECE: ESDM: Semi Conductor, Material Technology, Artificial Intelligence, Circuits Design and Fabrication			
	ITES: Blockchain, Quantum Computing			
Nodal Officer/PI/Contact Person	Dr Ashish Raman (ECE Department)			
	Email: ramana@nitj.ac.in			

D) Admission Procedure

- i. Shortlisting of the candidates will be based GATE score. Mere shortlisting of an applicant does not confirm admission to Ph.D. Programme. The admission shall be solely based upon the performance of individuals during "presentation and interaction" and availability of the Supervisor in the proposed area of research.
- ii. The Department Admission Committee for the ECE and IT Department shall recommend the suitable candidates for admission based on its assessment of presentation and interaction.
- iii. The Department Admission Committee/Institute reserves the right not to recommend any candidate for admission to PhD in the respective Department if the performance of the shortlisted candidates is not found satisfactory during "presentation and interaction". The decision of Department Admission Committee (approved by the competent authority of the Institute) shall be final.
- iv. The merit list of the selected candidates (based on presentation & interaction) shall be prepared on marks basis. A candidate who scores less than 40 marks (out of 100) for "presentation & interaction" shall not be considered "qualified" for admission to PhD programme and his/her name shall not be recommended for admission by Departmental Admission Committee.
- v. The list of recommended candidates for admission to PhD (Full-Time) programme shall be made in order of merit.
- vi. All the admitted candidates shall be governed by the PhD regulations of the Institute, guidelines of the Visvesvaraya PhD Scheme Phase –II funded by Ministry of Electronics and IT (MeitY) and other instructions issued by the Institute time to time as well as the Ministry of Electronics and IT (MeitY).

E) Other Issues

- i. Category (UR/EWS/OBC/SC/ST/PWD) once chosen by the applicant in his/her application form shall not be changed at a later stage. The candidate (s) applying under (EWS/OBC/SC/ST/PWD) category shall have to produce a valid category certificate issued by the competent authority.
- ii. OBC-NCL/EWS Certificate must have been issued on or after 1st April, 2025 so that the candidates from creamy layer are identified. No certificate issued before this date shall be acceptable.
- iii. All the candidates should ensure that they possess the required educational qualification by the last date of submission of the application under this Advertisement.
- iv. Certificate Checking: The certificates (in original) of all the candidates recommended for admission shall be checked by the individual Department before deposition of fee by the candidates.
- v. The candidate (in service) applying for full-time PhD programmes need to apply through proper channel. Any application without "No Objection Certificate" from the employer shall not be considered for shortlisting.
- vi. The application without proof of application fee as applicable/self-attested copies of

documents/certificates/testimonials shall be rejected and shall not be considered for shortlisting.

F) Fellowship

The candidates admitted under this Advertisement will be eligible for fellowship as mentioned in the Table at C) above. Fellowship shall be paid as per the guidelines of the Visvesvaraya PhD Scheme Phase –II funded by Ministry of Electronics and IT (MeitY) and other instructions issued by the Ministry of Electronics and IT (MeitY) in this regard. The period of the project is 05 years or till the completion of the project whichever is earlier. Fellowship will be started from the date of joining by the candidate in the Department and fellowship will be paid for a maximum duration of 05 Years or till the completion of project whichever is earlier (as per project guidelines).

H) Important Dates

Sr.	Activity	Date	
No.			
1.	Last date for submission of Applications	13/07/2025	
2.	Display of list of candidates eligible for presentation	14/07/2025	
	& interaction (GATE score)		
3.	Presentation/interaction by all eligible candidates	18/07/2025 at 10.00 AM	
4.	Display of list of selected candidates	18/07/2025	
5.	Deposition of fee & Registration	Till 21/07/2025	
6.	Commencement of classes	As notified by the	
		Department	

All the dates mentioned above are tentative subject to change at any stage by the competent authority. All the candidates interested in seeking admission are requested to visit the Institute website regularly for updates.

- I) All disputes pertaining to the admissions shall fall within the jurisdiction of Jalandhar only.
- **J)** All admissions will be provisional till these are confirmed subject to medical fitness, payment of all the fees, fulfillment of eligibility conditions, and verifications of certificates by the Academic Section of the Institute.
- **K)** After payment of fee (application/admission fee), no fee refund request shall be entertained in any case.
- L) The Institute reserves the right to modify or cancel this Advertisement/any part of this Advertisement at any stage.
- **M)** It is mandatory for all applicants to fill the preferences of prospective supervisors during the filling of applications. A separate link for the same will be displayed on the Institute Website.
- **N)** The list of the Faculties is available in the **Annexure-I**. Further, the candidates can view the research domain of the Faculties by visiting the Department Website from the Academics Menu of the Institute Website.

Annexure-I

Electronics and Communication Engineering					
Name Of Faculty	Working in	Emerging Area			
Prof Binod Kumar	ESDM	Antenna, Circuits Design and Fabrication			
Kanaujia Zasiri					
Dr Ashish Raman	ESDM	Semiconductor, Circuits Design and			
Prof. B S Saini	ESDM	AI			
Dr Mamta Khosla	ESDM	Semiconductor			
Dr Ramesh K Sunkaria	ESDM	AI			
Dr Nitesh Kashyap	ESDM	Circuits Design and Fabrication			
Dr Aijaz Mehdi Zaidi	ESDM	Antenna, Circuits Design and Fabrication			
Dr Asutosh Kar	ESDM	Circuits Design and Fabrication			
Dr Balwinder Raj	ESDM	Semiconductor			
Dr Bodile Roshan	ESDM	AI			
Dr. Rohit Singh	ESDM	AI, Communication			
Dr. Tarun Chaudhary	ESDM	Semiconductor			
Dr. Indu Saini					
	ESDM	AI, Communication			
Dr. Deepti Kakkar	ESDM	AI, Communication			
Dr. Sateesh Kumar	ESDM	AI, Communication			
Dr. Sukwinder Singh	ESDM	RF, Circuits Design and Fabrication,			
Dr. Kundan Kumar	ESDM	Antenna, Circuits Design and Fabrication			
Dr. Neetu Sood	ESDM	AI, Communication			
Dr. Pawan Kumar	ESDM	IOT			
Dr. Manjeet Singh	ESDM	AI, Communication			
Dr. Nitesh Kashyap	ESDM	Antenna, Circuits Design and Fabrication			
	Informa	tion Technology			
Name Of Faculty	Working in	Emerging Area			
Dr Vijay Kumar	ITES	AI, Quantam Computing			
Dr Mohit Kumar	ITES	AI			
Dr Nisha Chaurasia	ITES	AI, Quantam Computing			
Dr Avani Vyas	ITES	AI, BlockChain, Quantam Computing			
Dr Naveen Kumar Gupta	ITES	AI, BlockChain, Quantam Computing			
Dr. Kusum Kumari	ITES	AI, BlockChain, Quantam Computing			
Bharti	IILS	Hi, Blockenam, Quantum Computing			
Dr. Ranjeet Kumar	ITES	AI, BlockChain, Quantam Computing			
Dr. Simranjit Singh	ITES	AI, BlockChain, Quantam Computing			
Dr. Neeraj Kumar	ITES	AI, BlockChain, Quantam Computing			
Dr. Jaspal Kaur Saini ITES		AI, BlockChain, Quantam Computing			
Dr. Rabi Shaw ITES		AI, BlockChain, Quantam Computing			
Dr. Pallabi Sharma	ITES	AI, BlockChain, Quantam Computing			
Dr Vikas Chauhan ITES		AI, BlockChain, Quantam Computing			
Dr Bharat Krishan Mahaur	ITES	AI			